Topologies for High-Speed Drives

Giorgo Kapino
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Background

Giorgo Kapino

Ph.D. student in Power Electronics, Centre for Industrial Electronics – SDU

Topic: "Topologies for High-Speed Drives"

M.Sc. in Electronics, University of Southern Denmark

B.Sc. In Electrical Engineering, Technological Educational Institute of Central Greece

SDU Electrical Engineering

Overview

Motivation for high-speed drives

Topologies
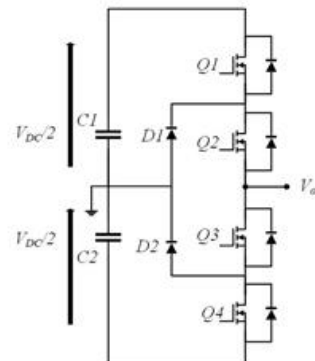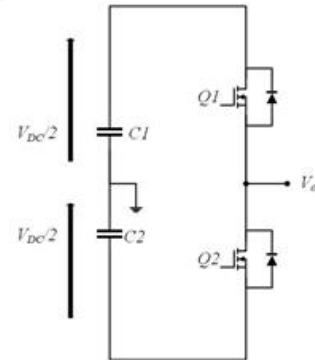
SiC die area characterization

Future plan
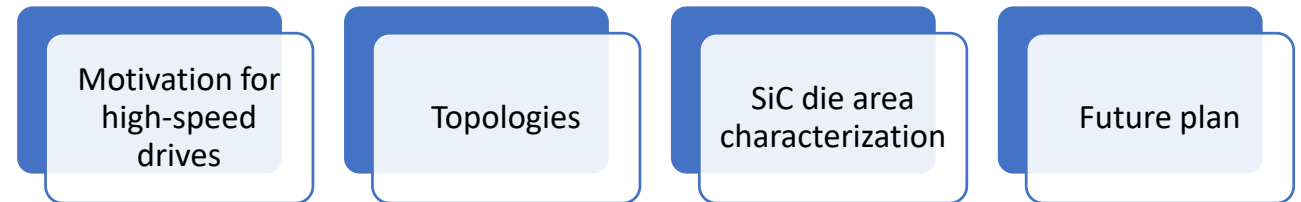
Motivation for High-Speed Drives
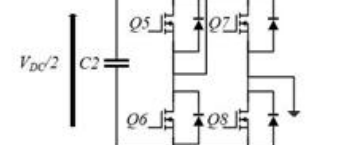
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Topologies

Traditional Two-level VSI

T-type NPC VSI

Flying Capacitor (FC) VSI

Neutral Point-Clamped (NPC) VSI

Active NPC VSI
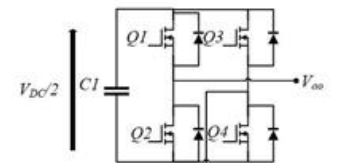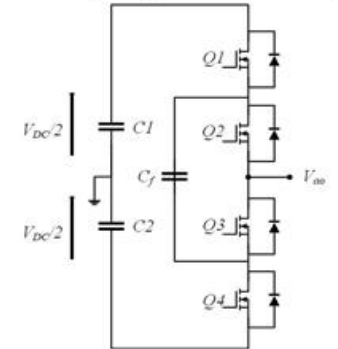
Cascaded H-bridge VSI

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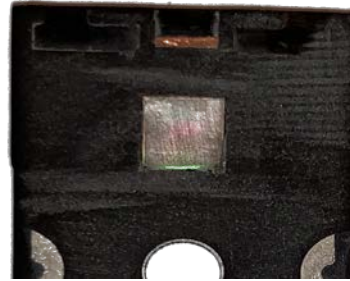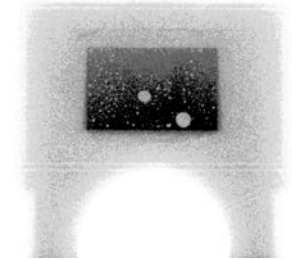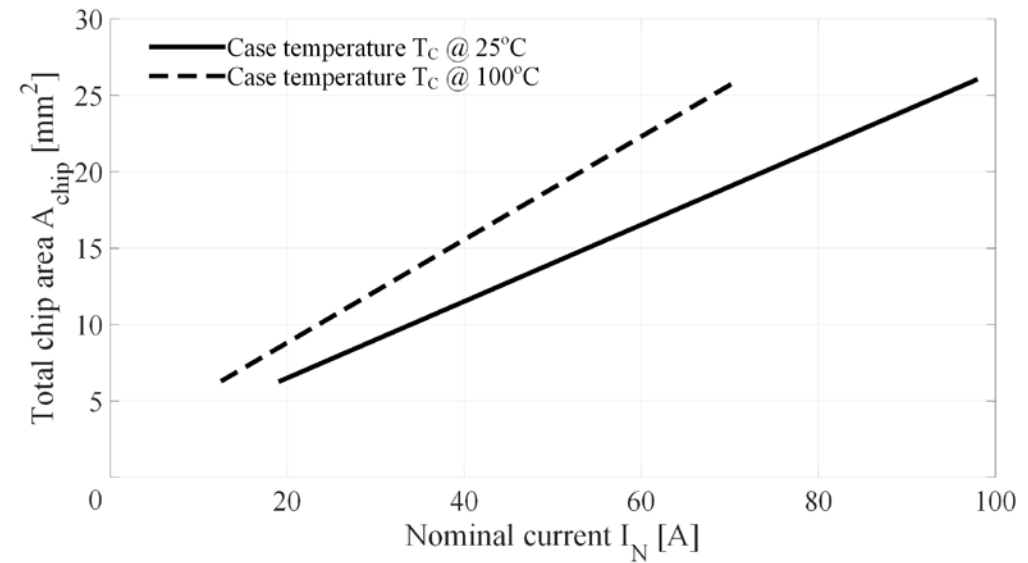# Efficiency comparison
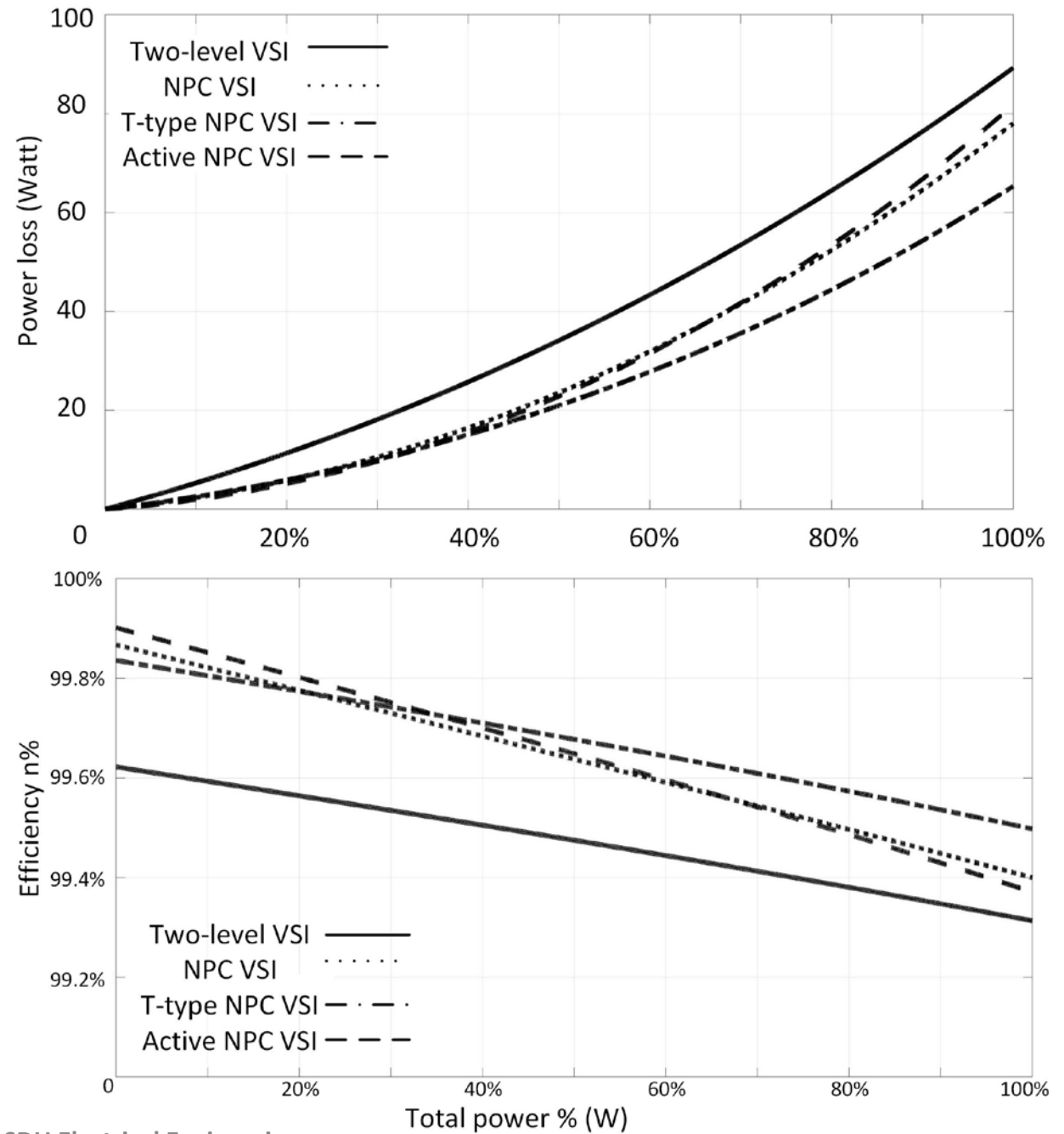
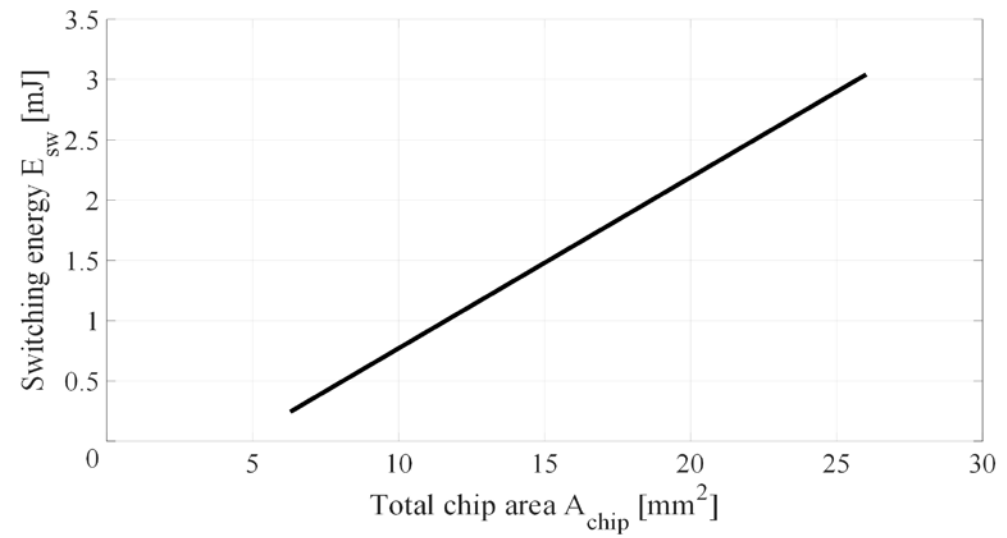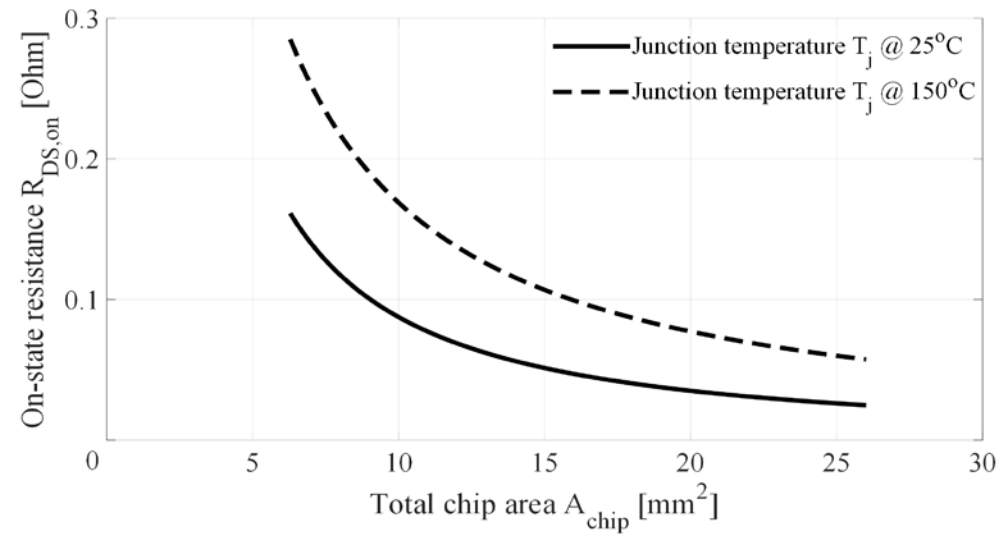# SiC die area characterization

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Rohm's SCT3030KL   Cree's C2M0025120D

SiC die area characterization

Future plan

Algorithm for iterative SiC chip area comparison

Prototype design

Filter design for high-speed drives

650V-900V SiC chip area characterization database

Thank you for your time. Questions?

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